REMARKS

The application has been amended and is believed to be in condition for allowance.

Claims 1-20 remain in this application.

Claim 12 has been amended to correct a typographic error.

Claim 15 has been amended responsive to the claim objection.

Withdrawal of the objection is solicited.

The independent claims are amended as described below. No new matter is entered.

Obviousness Rejections

The Official Action rejected claims 1-16 and 19-20 under 35 U.S.C. 103(a) as being unpatentable over CATALDO ("Net Processor Startup Takes Pipelined Path to 40 Gbits/s") in view of DORST (U.S. Patent Application 2004/0098549 A1) in view of HARRIMAN 6,330,645.

Claim 17 was rejected as obvious over CATALDO in view of DORST.

The below arguments apply to each of claims 1, 8, and 17. As to the arbiter, the arguments also apply to claim 19.

Claim 1 recites a processor; the parts are depicted in Figure 1 (reproduced below). External devices 140 are also

depicted, which external devices are located externally of the processor.

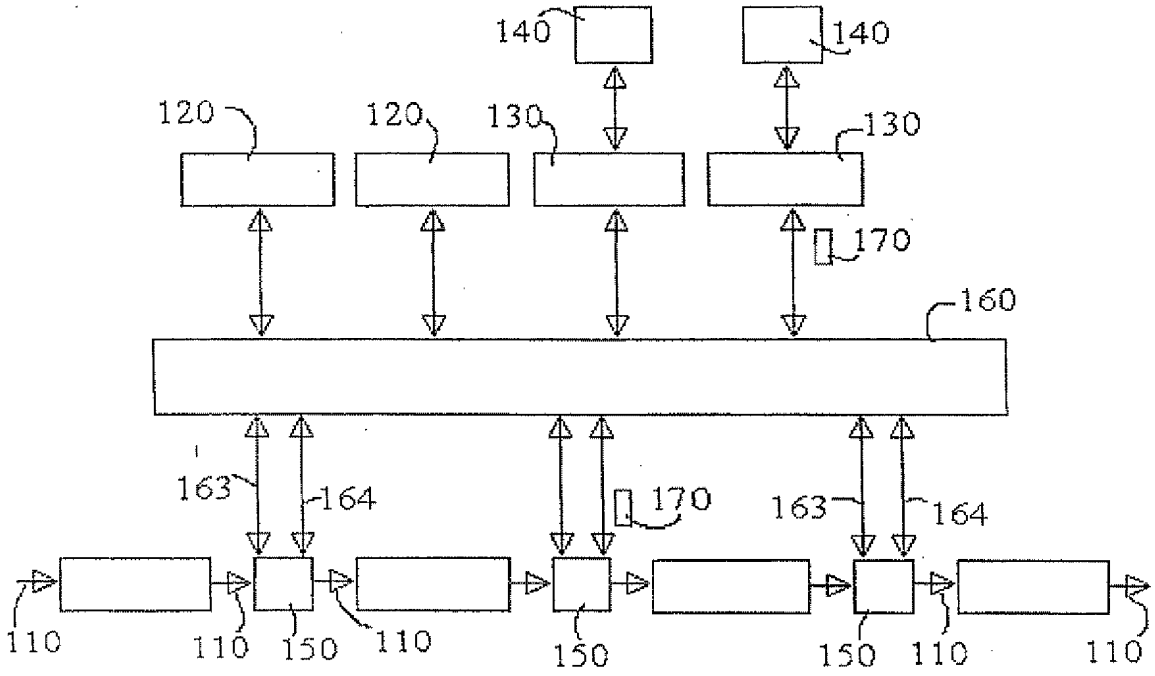

Fig. 1

Claim 1 recites "at least one interface engine adapted to be connected to at least one external device located externally of the processor;" Two interface engines 130 are shown, each connectable to respective external devices 140.

Claim 1 recites "a programmable pipeline adapted to directionally transfer data packets through the pipeline from a first end of the pipeline to a second end of the pipeline, and adapted to perform sequences of instructions on the data packets,". The programmable pipeline is depicted by the row of

blocks in the bottom of Figure 1, and its transfer of data packets is indicated in Figure 1 by the arrows 110.

Claim 1 also now recites "the pipeline comprising plural pipeline stages and plural access points, the pipeline stages and the access points being arranged in a row between the first end of the pipeline and the second end of the pipeline, the access points providing the at least one external device with access to the pipeline, at least one of the access points separating and connecting two of the pipeline stages,…".

These are illustrated as access points 150 separating the plural pipeline stages.

This recitation has been amended to make explicit that the connected access points provide the at least one external device with access to the pipeline. The significance of the access points, and the structural configuration is now believed to be more clearly recited. See the following recitation concerning the connection/interaction of the interface engine to/with the access points.

Claim 1 recites "wherein the at least one interface engine is connected to each of the plural access points,". The connections between the interface engines 130 and the access points 15 are exemplified as connections via a switch 160 and second channels 164 indicated by double arrows, (see also WO publication page 5 line 25 - page 6 line 8).

Claim 1 next recites that the at least one interface engine is adapted

i) to receive a request from any one of the connected access points of the programmable pipeline, the request being received upon arrival of one of the data packets at the respective any one access point,

ii) to send a request output to the external device, the request output being based at least partly on the request from the one access point,

iii) responsive to the request output, to receive an external reply from the external device, and

iv) to send to the pipeline a response, based on the external reply, to the request.

An example of a request from an access point 150 to an interface engine 130, upon arrival of a data packet to the access point, is depicted by a block 170. A request output to the external device is depicted with a block 270 in Figure 2, also showing details of an interface engine 130. An external reply from the external device is depicted with a block 330 in Figure 2, and a response based on the external reply is depicted with a block 340 in Figure 2.

Claim 1 concludes by reciting that "the interface engine includes an arbiter configured to allow forwarding of requests from the plural access points in a fair manner between each of the plural access points". An arbiter 190, adapted to

forward requests 170 from the access points in a fair manner, is shown in Figure 2 (showing details of an interface engine 130; see also WO publication page 6 lines 25-27).

As to claims 1 and 8, the Official Action states that CATALDO discloses a programmable pipeline adapted to directionally transfer data packets through the pipeline from a first end of the pipeline to a second end. The Official Action states that CATALDO inherently discloses plural access points located in a spaced apart relation between the first end of the pipeline and the second end of the pipeline.

The Official Action concedes that CATALDO does not disclose i) at least one interface engine, and ii) the arbiter as recited by claims 1 and 8.

The Official Action states that DORST discloses at least one interface engine as recited. The Official Action states that the teaching of DORST reduces the burden and overhead of processors interfacing with and controlling the memory and flexibly controls a multitude of memory circuits in a simple-to-use manner (OA page 5). The Official Action concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of DORST with the invention of CATALDO in order to reduce the burden and overhead of processors interfacing with and controlling the memory, as well as flexibly control a multitude of memory circuits in a simple-to-use manner (OA page 6).

HARRIMAN is offered (OA page 6) as disclosing an arbiter configured to allow forwarding of requests from plural access points in a fair manner between each of the plural access points (column 4, lines 19-40, arbiter 224, round robin scheme).

Notwithstanding the disclosure of each reference, applicants respectfully disagree that these references render obvious the recited invention.

CATALDO

As amended, the pipeline according to claim 1 comprises pipeline stages and access points arranged in a row, at least one of the access points separating and connecting two of the pipeline stages. Such pipeline stages are included in the rectangular blocks located between the access points 150 in the row of blocks in the bottom of Figure 1.

However, CATALDO does not disclose a pipeline stages separated and connected by access points as recited, where the access points provide external devices with access to the pipeline.

As the name indicates, the access points 150 provide access of the pipeline to devices external to the pipeline.

In contrast to the present invention, such external access is not even hinted in CATALDO.

This inventive feature was believed to be previously recited, see the recitation concerning the connection of the interface engine to the access points. However, this recitation

has been amended to make explicit that "the access points [are] providing the at least one external device with access to the pipeline".

On page 3 of the Official Action, the Examiner states that CATALDO inherently discloses access points, and the Examiner also states that the access points could simply be ports to each stage. Applicants respectfully disagree and point out that there is a significant difference between what must be a part of CATALDO and what might be a part of CATALDO.

In this regard, since CATALDO does not even discuss any device external to the pipeline, it cannot be understood why CATALDO would inherently discloses access points 150 connected to an interface engine 130.

CATALDO mentions that each pipeline stage acts as a mini-processor. On page 18 of the Official Action, the Examiner states that CATALDO teaches access points in that the processors, and access data that is transversing the pipeline. However, the Examiner has still not shown why the stages of CATALDO are access points 150 connected to an interface engine 130 to be connected to at least one external device located externally of the pipeline.

The Examiner has not shown that the recited structure is necessarily inherent to CATALDO. Thus, there is no basis for asserting the CATALDO makes this disclosure.

DORST

DORST discloses that several processors may share one memory controller, paragraph 0031. On pages 5 and 6 of the Official Action, the Examiner appears to indicate that memory controller of DORST corresponds to the interface engine of claim 1, and the processors of DORST can be seen as similar to the pipeline stages of CATALDO. However, as explained above, the access points of claim 1 are not the same as the pipeline stages of CATALDO.

On page 5 of the Official Action, the Examiner states that DORST also teaches multiprocessing and distributed processing systems (DORST paragraph 0036).

The Examiner seems to suggest that the pipeline of CATALDO is a form of distributed processing system. However, DORST simply suggests (paragraph 0036) concerning an embodiment where a data-processing block, comprising a processor and a memory controller, that such a block can be a node in a multiprocessor system or a node in a network of interconnected or distributed processors. Since each data-processing block contains a processor and a memory controller, which memory controller the Examiner wants to compare to an interface engine of claim 1, the embodiment of DORST in paragraph 0036 cannot be compared to an arrangement where a plurality of access points 150 are connected to an interface engine. Neither can the system nodes or network nodes of the embodiment of DORST in paragraph

0036 be compared to processing stages of the pipeline of CATALDO since these contain no memory controllers.

Therefore, DORST does not motivate the necessary modifications of CATALDO to provide the recited structure, absent the arbiter.

HARRIMAN

HARRIMAN is offered (OA page 6) as disclosing an arbiter configured to allow forwarding of requests from plural access points in a fair manner between each of the plural access points (column 4, lines 19-40, arbiter 224, round robin scheme).

The arbiter of the invention reduces risks of delays in the pipeline. This is now clearly recited in connection to the arbiter.

In the Office Action, under point 20, the Examiner provided arguments concerning the risk of delays.

However, it is not obvious to connect, as provided by the invention, external resources to a pipeline, due to the special circumstance that a delay at one part of the pipeline will affect the data traffic in other parts of the pipeline. This is a problem that is not addressed in any of the cited documents.

HARRIMAN discloses an arbiter at a memory controller with multiple requesters. However, the requesters are not part of a pipeline, and it is not critical in HARRIMAN for one requester that another requester receives a reply. This is

demonstrated by HARRIMAN suggesting (col. 4 lines 50-54) that the priority of a slow device is lowered if the slow device is requesting a relatively large amount of data. In contrast thereto, if an access point in a pipeline does not receive a request in time, the entire pipeline will be slowed down.

Thus, the scheme of HARRIMAN would not be adopted for a pipeline application.

Summary

For all the foregoing, it is respectfully submitted neither CATALDO nor DORST, individually or in combination, teach or suggest all the features recited in independent claims 1, 8, and 17, and that the further HARRIMAN reference fails to cure the defects of any fair CATALDO/DORST combination. Therefore, it is respectfully submitted that independent claims 1, 8, and 17, and all claims dependent therefrom, are patentable.

Reconsideration and withdrawal of the rejections are respectfully requested.

From the foregoing, it will be apparent that applicants have fully responded to the April 8, 2008 Official Action and that the claims as presented are patentable. In view of this, applicants respectfully request reconsideration of the claims, as presented, and their early passage to issue.

In order to expedite the prosecution of this case, it is requested that the Examiner telephone the attorney for

applicant at the number set forth below if the Examiner is of the opinion that further discussion of this case would be helpful.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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